CLAIM LISTING

This listing of claims will replace all prior versions, and listings of claims in the application:

AMENDMENTS TO THE CLAIMS

1. (Currently Amended) Apparatus for communicating data between a network transceiver and memory circuitry, comprising:

a transmit peripheral having a first streaming interface configured to receive a communication sequence having data read from said memory circuitry;

a receive peripheral having a second streaming interface configured to transmit a communication sequence having data to be written to said memory circuitry; and

media access control (MAC) circuitry configured to transmit said data read from said memory circuitry to said network transceiver, and receive said data to be written to said memory circuitry from said network transceiver.

2. (Original) The apparatus of claim 1, further comprising:

a bus bridge configured to receive control data from a processor, said control data operative to control said MAC circuitry.

3. (Original) The apparatus of claim 2, wherein said bus bridge is a device control register (DCR) bus bridge.

4. (Original) The apparatus of claim 1, wherein said communication sequence received by said transmit peripheral and transmitted by said receive peripheral comprises a header, a data section, and a footer.

5. (Original) The apparatus of claim 4, wherein said transmit peripheral comprises:

control logic for extracting control data from at least one of said header and said footer; and

checksum computation logic for computing checksum data for said data read from said memory circuitry in response to said control data.

6. (Original) The apparatus of claim 5, wherein said control data comprises checksum start offset data, checksum insert offset data, and checksum initial value data.

7. (Original) The apparatus of claim 5, wherein said control data is derived from a direct memory access (DMA) descriptor.

8. (Original) The apparatus of claim 5, wherein said transmit peripheral further comprises:

a checksum first-in-first-out (FIFO) memory for storing said checksum data; and

a data FIFO memory for storing said data read from said memory circuitry.

9. (Original) The apparatus of claim 4, wherein said receive peripheral comprises:

checksum computation logic for computing checksum data for said data to be written to said memory circuitry.

10. (Original) The apparatus of claim 9, wherein said receive peripheral comprises:

a checksum first-in-first-out (FIFO) memory for storing said checksum data; and

a data FIFO memory for storing said data to be written to said memory circuitry.

11. (Original) The apparatus of claim 9, further comprising:

control logic for inserting first control data into said header and second control data into said footer.

12. (Original) The apparatus of claim 11, wherein said data comprises a frame, and wherein said first control data comprises a length of said frame, and said second control data comprises said checksum data.

13. (Original) The apparatus of claim 12, wherein said first control data is disposed in a first direct memory access (DMA) descriptor in a chain of descriptors and said second control data is disposed in a last DMA descriptor of said chain of descriptors.

14. (Original) The apparatus of claim 1, wherein said data read from said memory circuitry and said data to be written to said memory circuitry comprises Gigabit Ethernet frames.

15. (Currently Amended) A method of communicating data between a network transceiver and memory circuitry, comprising:

receiving, over a streaming interface, a communication sequence from a direct memory access (DMA) controller configured to control said memory circuitry, said communication sequence having a header, a data section, and a footer, said data section including data read from said memory;

extracting control data from at least one of said header and said footer; and

computing checksum data for said data read from said memory circuitry in response to said control data.

16. (Original) The method of claim 15, further comprising:

buffering said data read from said memory circuitry and said checksum data; and

transmitting said data read from said memory circuitry and said checksum data to said network transceiver.

17. (Original) The method of claim 15, wherein said control data comprises checksum start offset data, checksum insert offset data, and checksum initial value data.

18. (Original) The method of claim 15, wherein said control data is derived from a direct memory access (DMA) descriptor.

19. (Cancelled)

20. (Currently Amended) A method of communicating data between a network transceiver and memory circuitry, comprising:

transmitting, over a streaming interface, a communication sequence to a direct memory access (DMA) controller configured to control said memory circuitry, said communication sequence having a header, a data section, and a footer, said data section including data to be written to said memory circuitry;

computing checksum data for said data to be written to said memory circuitry;

inserting first control data into said header; and

inserting second control data into said footer.

21. (Original) The method of claim 20, further comprising:

receiving said data to be written to said memory circuitry from said network transceiver; and

buffering said data to be written to said memory circuitry and said checksum data.

22. (Original) The method of claim 20, wherein said data to be written to said memory circuitry comprises a frame, and wherein said first control data comprises a length of said frame, and said second control data comprises said checksum data.

23. (Original) The method of claim 20, wherein said first control data is disposed in a first direct memory access (DMA) descriptor in a chain of descriptors and said second control data is disposed in a last DMA descriptor of said chain of descriptors.

24. (Cancelled)

25. (Currently Amended) A data communications system, comprising:

a network transceiver for communicating data using a protocol;

a processor for executing a protocol stack associated with said protocol;

memory circuitry;

a direct memory access (DMA) controller for controlling said memory circuitry; and

a media access controller (MAC), coupled to said DMA controller ~~by a streaming interface,~~ said MAC comprising:

a transmit peripheral having a first streaming interface configured to receive a communication sequence from said DMA controller ~~over said streaming interface~~, said received communication sequence having data read from said memory circuitry;

a receive peripheral having a second streaming interface configured to transmit a communication sequence to said DMA controller ~~over said streaming interface~~, said transmitted communication sequence having data to be written to said memory circuitry; and

MAC circuitry configured to transmit said data read from said memory circuitry to said network transceiver, and receive said data to be written to said memory circuitry from said network transceiver.

26. (Original) The system of claim 25, wherein said protocol comprises a Gigabit Ethernet protocol.

27. (Original) The system of claim 25, wherein said MAC further comprises:

a bus bridge configured to receive control data from said processor, said control data operative to control said MAC circuitry.

28. (Original) The system of claim 27, wherein said bus bridge comprises a device control register (DCR) bus bridge.

29. (Original) The system of claim 25, wherein said communication sequence received by said transmit peripheral and transmitted by said receive peripheral comprises a header, a data section, and a footer.

30. (Original) The system of claim 29, wherein said transmit peripheral comprises:

control logic for extracting control data from at least one of said header and said footer; and

checksum computation logic for computing checksum data for said data read from said memory circuitry in response to said control data.

31. (Original) The system of claim 29, wherein said receive peripheral comprises:

checksum computation logic for computing checksum data for said data to be written to said memory circuitry; and

control logic for inserting first control data into said header and second control data into said footer.